Please add th following new claim:

B4

25. The circuit of claim 1, wherein said differential sense circuit is coupled to said latch in a push-pull configuration.

REMARKS

The above-referenced patent application has been reviewed in light of the Office Action, dated April 16th, 2002, in which: Claims 5 and 6 are rejected under 35 U.S.C. 112, second paragraph; claims 1, 3-6 and 11-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Takahashi (hereinafter "Takahashi (824)", US Patent No. 6,037,824); claims 7 and 17-24 are rejected under 35 U.S.C 103(a) as being unpatentable over Takahashi (824); claims 17-20 are rejected under 35 U.S.C 103(a) as being unpatentable over Takahashi (hereinafter "Takahashi (689)", US Patent No. 5,982,689) and further in view of Takahashi (824). Reconsideration of the above-referenced patent application in view of the foregoing amendments and following remarks is respectfully requested.

Claims 1 and 3-25 are now pending the above-referenced patent application. Claims 1, 5 and 17 have been amended, claim 25 has been added, and no claims have been cancelled. It is noted that claims 1 and 17 have been amended back to their original scope, and claim 25 has been added to replace previously cancelled claim 2. These claims had been amended and/or cancelled in order to expedite prosecution of this patent application, however, because prosecution has not been significantly expedited, Applicants wish to return to the original scope of these claims, a scope to which they believe they are entitled in light of the prior art cited by the Examiner. It is respectfully asserted that there is, thus, no narrowing in scope or any prosecution history estoppel present as a result of these amendments.

The Examiner has reject d claims 5 and 6 under 35 U.S.C. 112, second paragraph. Applicants have amended claim 5, and it is respectfully asserted that claim 5 is in a condition for

allowance. It is noted that the amendment to claim 5 is made to address some of the concerns of the Examiner. How ver, these formal amendments do not narrow the scope of claim 5 as it was originally presented. Therefore, these amendments do not produce any prosecution history estoppel, nor has there been any surrender of claimed subject matter as a result Claim 6 depends from claim 5, and it is respectfully asserted that claim 6 is, therefore, also in a condition for allowance.

The Examiner has rejected claims 1, 3-6 and 11-16 under 35 U.S.C. 102(e) as being anticipated by Takahashi (824). This rejection is respectfully traversed. It is also respectfully asserted that the foregoing claims, as amended, are in a condition for allowance.

It is well-established that in order to establish a *prima facie* case of anticipation under 102 of the patent statute, the Examiner must a provide prior art document that meets each and every element and limitation of the rejected claim. Therefore, even if a single element or limitation is not met by the asserted document, then the Examiner has not succeeded in establishing a *prima facie* case.

Applicants begin with claim 1. Claim 1, as amended, recites:

" A circuit comprising:

a differential sense circuit;

a latch;

said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle."

According to the Examiner, "Regarding claim 1, figure 7 of Takahashi shows a circuit comprising: a differential sense circuit (210, 220, 231); a latch (233); said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in the latch is retained for at least one clock cycle, wherein said differential sens circuit is coupled to said latch in a push-pull (P31, N31, P32, N32)."

It is respectfully asserted that Takahashi (824) does not recite all of the elements of claim 1, as amended. As just an example, Takahashi (824) does not disclose a differential sense latch, and the elements disclosed in the Takahashi (824) patent do not contain the same elements as the differential sense latch claimed by Applicants. Figure 7 of Takahashi (824) discloses a sense amplifier coupled to a latch consisting of cross-coupled NAND gates. However, claim 1 recites, instead, a differential sense circuit and a latch coupled to form a differential sense latch.

In fact, Applicants disclosed the particular configuration of FIG. 7 of Takahashi (824) as prior art in the detailed description at page 5, lines 4-12. Quoting from the detailed description, page 5, lines 26-29, "For example, because of the cross-coupled configuration of the latches employed in these embodiments, two full CMOS gate delays would be added to a signal path in which such a latch is employed. These gate delays may, therefore, adversely affect the performance of such a signal path."

As demonstrated by the particular embodiment disclosed in the patent application, a differential sense latch as recited in claim 1 provides performance advantages over the prior art of FIG. 7 Takahashi (824) or Figure 1 of the above referenced patent application. It is noted, of course, that claim 1 is not limited to only the particular embodiment shown. However, it is respectfully asserted that not only has the Examiner not made a *prima facie* case of anticipation under 102 of the patent statute, but the differential sense latch as claimed by Applicants solves a problem inherent in the design disclosed in Takahashi (824).

Furthermore, the Examiner states, "Applicant never describes the structure of the latch of claim 1. Applicant is respectfully reminded that a claim is considered based on the recited elements and its language." (emphasis omitted). Although Applicants respectfully disagree, the foregoing is believed sufficient to overcome the rejections of the Examiner. Nonetheless, Applicants reserve the right address this argument at a later time if Applicants believe it is warranted.

Claims 3-6 and 10 depend upon and include all limitations of claim 1, and patentably distinguish from Takahashi (824) for at least the same reasons as claim 1. It is, therefore, respectfully asserted that claims 3-6 are in a condition for allowance.

Claim 11 patentably distinguishes from the cited patent for at least reasons similar to claim 1. It is, therefore, respectfully asserted that claim 11 is in a condition for allowance.

Claims 12-16 depend from and include all limitations of claim 11. It is respectfully asserted that claims 12-16 patentably distinguish from Takahashi (824) for at least the same reasons as claim 11, and are, therefore, in a condition for allowance.

The Examiner has rejected claim 7 and 17-24 under 35 U.S.C. 103(a) as being unpatentable over Takahashi (824). The rejection of these claims by the Examiner is respectfully traversed.

According to the Examiner, "[F]igure 7 of Takahashi (824) includes all of the limitations of the present invention except for the limitation that the sense amplifier comprises an n-type sense amplifier. However, it is well known in the art that the n-type or the p-type sense amplifier is used depending on the selection of supply voltages to make them conductive. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to use the n-type sense amplifier to conform to the 'high level' input signals." However, the elements of the Takahashi (824) patent cited by the Examiner fail to make a *prima facie* case of obviousness under the patent statute.

It is well-known that in order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the Examiner must show a suggestion or motivation, either in the references themselves or in knowledge generally available to one of ordinary skill in the art, to modify a prior art reference or combine two or more prior art references. Second, the Examiner must show a reasonable expectation of success in making this combination or modification. Third, the Examiner must show that the combination or modification, if proper, contains all of the elements of the application under examination. If any of these elements are not met, the

Examiner has failed to establish a successful *prima facie* case of obviousness. It is respectfully asserted that the Examiner has failed to establish a prima facie case of obviousness in regard to this claim.

As just an example, the Takahashi (824) patent fails to recite all of the elements of claim 7. It is noted that claim 7 depends from and includes all limitations of claim 1, as amended. As stated previously in reference to claim 1, Takahashi (824) does not disclose a differential sense latch as claimed by Applicants. Figure 7 of Takahashi (824) discloses a sense circuit, and a latch consisting of cross-coupled NAND gates. As is clear from claim 1, a differential sense latch includes a differential sense circuit and a latch, which do not appear to be illustrated in Figure 7 of Takahashi (824). It is respectfully asserted that the Examiner has not even cited a combination of prior art documents that together contain all the elements of claim 7, as amended. As stated in *In re Kotzab, 217 F.3d 1365, 1370 (Fed. Cir. 2000)*, "[e]ven when obviousness is based on a single prior art reference, there must be a showing of suggestion or motivation to modify the teachings of that reference." Additionally, as stated in MPEP 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Here, no such suggestion or motivation has been demonstrated, therefore, claim 7, as amended, is in condition for allowance.

Claim 17 distinguishes from the cited patent at least for reasons similar to those made in reference to claim 7. As just an example, Takahashi (824) does not disclose a differential sense latch as claimed. Applicants rely at least in part on arguments previously made in reference to claim 7, above. It is, therefore, respectfully asserted that claim 17 is in a condition for allowance.

Claims 18-24 depend from and include all limitations of claim 17. It is, therefore, respectfully asserted that these claims are in a condition for allowance.

The Examiner has rejected claims 17-20 under 35 U.S.C. 103(a) as being unpatentable over Takahashi (689) further in view of Takahashi (824). The rejection of these claims by the Examiner is respectfully traversed.

According to the Examiner, "[F]igure 1 of Takahashi (689) show an integrated circuit (IC) comprising: a plurality of data paths, at least one of said data paths comprising: a differential circuit (SA) and a differential sense latch (CELL, M31, M41, M11, M21), wherein said differential sense latch comprises a differential sense circuit (M31, M41, M11, M21) and a jam-latch (CELL) coupled such that, in operation, an electronic signal based, at least in part, on differential output terminals of said differential circuit is stored in said jam-latch; not disclosed is the differential sense circuit is coupled to said jam-latch in a push-pull configuration. Figure 7 of Takahashi (824) teaches a differential circuit (210), and a differential sense latch (231, 232, 233) wherein the differential sense circuit (231, 232) is coupled to the latch (233) in a push-pull configuration..."

Contrary to the Examiner's opinion, the cited patents do not establish a *prima facie* case of obviousness, or even show or describe all of the elements of the rejected claims. As just an example, and as stated previously, Takahashi (824) does not disclose a differential sense circuit as claimed by Applicants. The differential sense latch as claimed by Applicants solves a problem inherent in the design disclosed in Takahashi (824). It is respectfully asserted that even if the combination of Takahashi (689) with Takahashi (824) were proper, although Applicants believe that it is not, it would still fail to meet all of the elements of the rejected claims. Therefore, it is respectfully asserted that claims 17-20 are in a condition for allowance.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all claims in this application, as amended, are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (503) 264-9427. Reconsideration of this patent application and early allowance of all the claims, as amended, is respectfully requested.

Respectfully submitted,

Michael J. Willardson
Patent Agent
Reg. No. 50,856

Dated: 10/15/02

c/o Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA 90025-1026
(503) 264-0967

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October 15, 2002
Date of Deposit

Angie C. Farr
Name of Person Mailing Correspondence

Angie C. Farr 10.15.02
Signature *Date*

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims have been amended as follows:

1. (twice amended) A circuit comprising:

a differential sense circuit;

a latch;

said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle~~, wherein said differential sense circuit is coupled to said latch in a push-pull configuration~~.

5. (once amended) The circuit of claim 4, wherein said differential sense circuit comprises:

a first inverter and a second inverter, said first and second inverters having an input terminal and an output terminal, said input terminal of said first and second inverter being coupled respectively to a pull-down terminal, said output terminal of said first and second inverter being coupled respectively to a pull-up terminal~~, said a pull-up terminal and a pull-down terminal;~~, said output terminals of said first and second inverter being respectively coupled to opposite terminals of said latch, said input ~~pull-down~~ terminals of said first and second inverter being respectively coupled to a non-inverted output terminal and an inverted output terminal of said p-type sense amp;

a third inverter having an input terminal and an output terminal, said input terminal being coupled to said inverted output terminal and said output terminal being coupled to said pull-up terminal coupled to ~~of~~ said first inverter; and

a fourth inverter having an input terminal and an output terminal, said input terminal being coupled to said non-inverted output terminal and said output terminal being coupled to said pull-up terminal coupled to ~~of~~ said second inverter.

17. (twice amended) An integrated circuit (IC) comprising:

a plurality of datapaths, at least one of said datapaths comprising:

a differential circuit and a differential sense latch, wherein said differential sense latch comprises a differential sense circuit and a jam-latch coupled, such that, in operation, an electronic signal based, at least in part, on differential output terminals of said differential circuit is stored in said jam latch~~, wherein said differential sense circuit is coupled to said jam latch in a push-pull configuration~~.

25. The circuit of claim 1, wherein said differential sense circuit is coupled to said latch in a push-pull configuration.